

Sigasi.[®]



Modern VHDL design

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Talk: “Bringing the power of Eclipse to VHDL designers”: Thursday, 14:15

- Hardware designers use simple editors
- Digital design is hard and error prone
- Software guys have much better tools

VHDL - tutorial/testbench.vhd - Sigasi - /Users/philippe.faes/workspaceSigasi

Project Expl

- tutorial [work]
 - Common Libraries
 - clock_generator.vhd [work]
 - dut.vhd [work]
 - testbench.vhd [work]

```

7
8 architecture STR of testbench is
9     signal data_out : std_logic_vector(7 downto 0);
10    signal data_in  : std_logic_vector(7 downto 0);
11    signal valid    : std_logic;
12    signal new_name_for_start : std_logic;
13    signal clock    : std_logic;
14    signal reset    : std_logic;
15    constant PERIOD : time := 50 ns;    -- Half the clock period. The fr
16
17 begin
18     clock_generator_instance : entity work.clock_generator(BEH)
19         generic map(
20             PERIOD => PERIOD
21         )
22     port map(
23         clock => c
24     );
25

```

PERIOD = 50 ns
 PERIOD : constant time
 Half the clock period. The frequency will be $1/(2*PERIOD) = 100$ MHz

Outline

- testbench.vhd
 - Entity : work.testbench
 - Architecture : work.testbench
 - Declarations
 - data_out : sign

Hierarchy

Top: work.testbench

- work.testbench(STR)
 - clock_generator_in
 - CLOCK_DRIVER
 - dut_instance: work
 - OUTPUT GENER

Problems

0 errors, 1 warning, 0 others

Description	Resource	Path	Location	Type
Warnings (1 item)				
Unused declaration	dut.vhd	/tutorial	line: 16 /tuto...	VHDL check (...

0 items selected

- **Type time compiler**
- Direct feedback
- Read output of other tools (ModelSim, ...)
- IDE *thinks* along

- Intelligent navigation
- Instant error reporting (faster feedback)
- Intelligent code completion
- Linting + Quick Fix
- Automated compile step
- All features work, even if code is **incomplete** (important for legacy projects)

Customers worldwide, in healthcare, telecom, consumer electronics, industrial automation, automotive, aerospace and defense.



- Sigasi 2.x Starter Edition
 - free
- Sigasi 2.x Pro
 - € 600 / license / year
 - Floating or node locked
- Training & Support
 - custom
- Available as plugin and stand-alone

Custom add-ons:

- Integration with tool flow
- Code review tool
- Style guide checker
- Project templates / code templates
- Issue tracker, Version control system
- . . .

- VHDL
- Build on Eclipse technology (Xtext, EMF, ...)
- Commercial, closed source